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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,188	03/01/2004	Reed A. Linde	42P15390	3180

8791 7590 11/15/2005

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EXAMINER	
TRAN, MICHAEL THANH	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/791,188	LINDE ET AL.
	Examiner	Art Unit
	Michael t. Tran	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-26 and 28-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,11-14,20,24-26,28 and 31* is/are rejected.

7)☒ Claim(s) *7-10,15-19,21-23,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *061705*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

MICHAEL TRAN
PRIMARY EXAMINER

DETAILED ACTION

1. In response to the Communications dated August 29, 2005, claims 1-4, 6-26, and 28-31 are active in this application as a result of the cancellation of claims 5 and 27.

Claim Objections

2. Claims 4, 7-10, 15-19, 21-23, 29, and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections – 35 U.S.C. § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1-3, 6, 11, and 12 are rejected under 35 U.S.C 102(b) as being

anticipated by Naganawa [U.S. Patent #6,219,280].

With respect to claim 1, Naganawa discloses, in figure 4 and column 10, a method comprising: detecting an electrical characteristic identifying a defect in a memory unit [s200]; and replacing the memory unit with an alternate memory unit [s40], wherein the replacing is performed during user operation [testing by tester – see column 10] of a device having the memory unit and the alternate memory unit; wherein the detecting is performed during an erase operation [erase – verify – s200].

With respect to claim 2, Naganawa discloses, in columns 5-7, that the detecting the electrical characteristic comprises: monitoring a current during an erase attempt; and identifying the defect when the current passes a predetermined current threshold [4th paragraph of the "Description of the Preferred Embodiments" section].

With respect to claim 3, Naganawa discloses, in columns 5-7, that the detecting the electrical characteristic comprises: monitoring a voltage during an erase attempt; and identifying the defect when the voltage passes a predetermined voltage threshold [2nd paragraph of the "Description of the Preferred Embodiments" section].

With respect to claim 6, Naganawa discloses, in column 1, lines 30-40, that the replacing the memory unit with the alternate memory unit comprises: causing the memory unit to be un-accessible at a memory address; and causing the alternate memory unit to be accessible at the memory address [defective memory cell is replaced with a redundant memory cell upon an access to this address].

With respect to claim 11, Naganawa discloses, in column 1, lines 1-15, that the memory relates to a nonvolatile memory. It is well known in the art that a flash memory is a nonvolatile memory.

With respect to claim 12, Naganawa discloses, in column 1, lines 1-15, that the memory relates to a nonvolatile memory. It is well known in the art that a flash memory has a plurality of rows and columns and that it is a nonvolatile memory.

5. Claim 14 is rejected under 35 U.S.C 102(b) as being anticipated by Naganawa [U.S. Patent #6,219,280].

With respect to claim 14, Naganawa discloses, in figures 3 and 4, an apparatus comprising: a plurality of accessible memory units [within 1]; one or more redundant memory units [within 2]; a failure detection unit [7] coupled to the plurality of accessible memory units [via 6] configured to monitor electrical characteristics in the plurality of accessible memory units during an erase operation and detect an electrical characteristic that identifies a defect in one of the plurality of accessible memory units [s200]; and a redundant block swap unit [3] coupled to the plurality of accessible memory units [via 4] and the one or more redundant memory units, the redundant block swap unit configured to replace to the one of the plurality of accessible memory units with one of the one or more redundant memory units.

6. Claim 20 is rejected under 35 U.S.C 102(e) as being anticipated by Santin

[U.S. Patent #6,847,574].

With respect to claim 20, Santin discloses, in figures 1, 2, and 5, a system comprising: a processor [506]; an antenna [504] coupled to the processor; and a memory device [508 – flash memory] coupled to the processor, the memory device comprising: a plurality of accessible memory units [110 of flash memory 100 of figure 1]; one or more redundant memory units [108]; a failure detection unit [within 108 – see column 1, lines 25-40] coupled to the plurality of accessible memory units configured to monitor electrical characteristics in the plurality of accessible memory units and to detect an electrical characteristic that identifies a defect in one of the plurality of accessible memory units; and a redundant block swap unit [106] coupled to the accessible memory units and the one or more redundant memory units, the redundant block swap unit configured to replace the one of the plurality of accessible memory units with one of the one or more redundant memory units.

7. Claims 24-26, 28, and 31 are rejected under 35 U.S.C 102(b) as being anticipated by Naganawa [U.S. Patent #6,219,280].

With respect to claim 24, Naganawa discloses, in figures 3, 4 and column 10, an apparatus comprising: a computer readable medium [figure 3]; and instructions stored on the computer readable medium [figure 4] to: detect an electrical characteristic that identifies a defect in a memory unit [s200]; and replace the memory unit with an alternate memory unit [s40], wherein the replacing is performed during user operation [testing by tester – see column 10] of a device having the memory unit and the

alternate memory unit; wherein the detecting is performed during an erase operation [erase – verify – s200].

With respect to claim 25, Naganawa discloses, in columns 5-7, that the instructions to detect the electrical characteristic comprises instructions to: monitor a current; and identify the defect when the current exceeds a predetermined current threshold [4th paragraph of the "Description of the Preferred Embodiments" section].

With respect to claim 26, Naganawa discloses, in columns 5-7, that the instructions to detect the electrical characteristic comprises instructions to: monitor a voltage during an erase attempt; and identify the defect when the voltage exceeds a predetermined voltage threshold [2nd paragraph of the "Description of the Preferred Embodiments" section].

With respect to claim 28, Naganawa discloses, in column 1, lines 30-40, that the instructions to replace the memory unit with the alternate memory unit comprises instructions to: cause the memory unit to be un-accessible at a memory address; and cause the alternate memory unit to be accessible at the memory address [defective memory cell is replaced with a redundant memory cell upon an access to this address].

With respect to claim 31, Naganawa discloses, in column 1, lines 1-15, that the memory relates to a nonvolatile memory. It is well known in the art that a flash memory is a nonvolatile memory.

Claim Rejections – 35 U.S.C. § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 13 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Naganawa [U.S. Patent #6,219,280] in view of Gudesen et al. [U.S. Patent # 6,380,597].

Naganawa discloses, in figure 4 and column 10, a method comprising: detecting an electrical characteristic identifying a defect in a memory unit [s200]; and replacing the memory unit with an alternate memory unit [s40], wherein the replacing is performed during user operation [testing by tester – see column 10] of a device having the memory unit and the alternate memory unit; wherein the detecting is performed during an erase operation [erase – verify – s200].

Naganawa discloses all of the above mentioned but is silent about the fact that the memory contain row of polymer memory. However, column 3, lines 10-25, shows that it is well known and desirable to have memory based polymer materials. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Naganawa memory circuit element to include a memory elements made of polymer materials as taught by Gudesen et al., since Gudesen et al. show that it is well known and cost effective in the art to provide a memory circuit elements made of polymer materials to store data.

Allowable Subject Matter

10. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- Programming address status bits of the alternate memory unit with the memory address.
- Setting a used status bit of the alternate memory unit.
- The failure detection circuit comprising: a current detection unit to detect a current during the erase operation.
- The failure detection circuit comprising: a voltage detection unit to detect a voltage during the erase operation.
- The failure detection circuit comprising: a resistance detection unit to detect a resistance during the erase operation.
- Wherein the redundant block swap unit is configured to program the address status bits and the used status bit to cause the plurality of memory cells to be accessible.

Conclusion

11. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

12. Any inquiry concerning this communication or earlier communications from

the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

13. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
November 10, 2005

MICHAEL TRAN
PRIMARY EXA